REMARKS

Claims 13-25, 27, 29, 32 and 35 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite. Applicants respectfully disagree that the features of the notification device and the device control unit as recited in the claims are "contradictory." Nevertheless, independent claims 13, 27, 29, 32 and 35 have been further amended to overcome this rejection. Withdrawal of the rejection is respectfully requested.

Claims 13-23, 27, 29, 32 and 35 stand rejected under § 102(b) on the basis of Bouvier et al. Applicants respectfully traverse this rejection because the cited reference does not disclose (or suggest) that a determination that a failure has occurred in a device and the use of the device is prohibited is made independent of the device control unit that performs control over the failed device.

The Bouvier et al. reference discloses a processor failure detection and recovery a circuit 240 including a control circuit 250 for resetting both processing units 202 and 204 at the initial power on or reset of the system 200. A registry unit 256 detects occurrences of various types of failures of the processing unit 22 following the reset initiated by the control unit 250 (see e.g., col. 5, line 65 to col. 6, line 29). As such, the control unit that controls the processor units 202 and 204 is a part of the system for determining a failure in processing units.

In the present invention, in contrast, a determination that a failure has occurred in a device is made independent of a device control unit that performs control over the failed

device. For this reason, independent claims 13, 27, 29, 32 and 35, and dependent claims 14-25 are allowable over the cited reference.

Claims 26, 28, 30, 33 and 36 stand rejected under § 102 on the basis of Jippo et al. Applicants respectfully traverse this rejection because the cited reference does not disclose (or suggest) the features of the notification device for notifying a second system, which is external to the first system, of the prohibition of use of the failed device and other devices in the first system, as described in claims 26, 28, 30, 33 and 36.

The fault recovery processor 17 of Jippo et al. includes a feature for checking a valid/invalid code assigned to each of the arithmetic processors 15 to determining whether vector pipelines 24-27 for each of the processors are to be isolated from the computer (which comprises all the components of Fig. 1) or whether each of the arithmetic processors is to be isolated as a whole from the computer (see col. 2, lines 24-30). Thus, the Jippo et al. reference teaches that the isolation of the arithmetic processors is done entirely within a single computer system. However, the reference does not disclose (or suggest) a feature for notifying a second system, which is external to the system, of the prohibition of use of the failed device in the first system, as now described in claims 26, 28, 30, 33 and 36. For this reason, these claims are now allowable over the cited reference.

Claims 24 and 25 stand rejected under §103(a) as being unpatentable over Bouvier in view of Fuss et al. Applicants respectfully traverse this rejection for the reasons given with respect to claim 13, from which these claims depend, and because of the additional features recited in these claims.

For the foregoing reasons, applicants believe that this case is in condition for allowance, which is respectfully requested. The examiner should call applicants' attorney if an interview would expedite prosecution.

Respectfully submitted,

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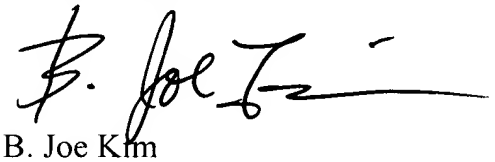
By 

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